IN THE CLAIMS:

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

Please CANCEL claims 6-14, without prejudice.

1. (ORIGINAL) An integrated circuit device having a send/receive macro for serially transferring addresses and data to or from an external device via a serial transfer bus, the integrated circuit device comprising:

a CPU for performing predetermined processing, wherein

the send/receive macro comprises:

a send/receive buffer accessed by the CPU, for storing a plurality of units of data to be transmitted to or received from the serial transfer bus;

an acknowledge detection unit for detecting a data acknowledge signal transmitted from a receiving device in response to transmission of predetermined units of data; and

a data send unit for transmitting data stored in the send/receive buffer, in response to detection of the data acknowledge signal by the acknowledge signal detection unit, without generating any interrupt to the CPU, and wherein

the acknowledge detection unit generates a data acknowledge signal non-detection interrupt to the CPU if the acknowledge detection unit does not detect the data acknowledge signal transmitted from the receiving device in response to transmission of the predetermined units of data.

2. (ORIGINAL) The integrated circuit device according to claim 1, wherein

the data transmission from the data send unit is terminated in response to the data acknowledge signal non-detection interrupt to the CPU.

3. (ORIGINAL) The integrated circuit device according to claim 1, wherein

when an address acknowledge signal is detected that is sent by a slave device in response to a transmission of an address identifying the slave device by the data send unit as a master, the acknowledge detection unit generates an interrupt to the CPU.

4. (ORIGINAL) The integrated circuit device according to claim 1, wherein the data send unit initiates serial transmission of predetermined units of data stored in the send/receive buffer, after an interrupt to the CPU generated when the acknowledge detection unit detects the address acknowledge signal.

5. (ORIGINAL) The integrated circuit device according to claim 1, wherein the serial transfer bus comprises a single data line and a single clock line, and wherein the data transfer is carried out serially over the single data line in synchronization with a clock driven onto the clock line.

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